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| **Project2 Details** |

Implement a MIPS simulator that can perform the following steps:

* load a specified MIPS text file.
* perform pipelined simulation and print the register/buffer/memory contents.

Please check this page often and make sure you see all the announcements.   
Detailed Instructions are available here: [Project2 (PDF)](http://www.cise.ufl.edu/class/cda5155sp12/projects/Project2/project2.pdf).   
  
The sample input/output files are given below:

* [sample.txt](http://www.cise.ufl.edu/class/cda5155sp12/projects/Project2/sample.txt): This is the input to your program.
* [simulation.txt](http://www.cise.ufl.edu/class/cda5155sp12/projects/Project2/simulation.txt): This is what your program should output as simulation trace.
* You can also view the [disassembly.txt](http://www.cise.ufl.edu/class/cda5155sp12/projects/Project2/disassembly.txt) for the above input file. This is for your reference only.

Correct handling of the sample code (with possible different data values) will be used to determine 60% of credit awarded. The remaining 40% will be determined from other test cases that you will not have access prior to grading. It is recommended that you construct your own sample input files with which to further test your pipelined processor simulation.

The following new test case was used in grading Project 2:

* [t1.txt(input)](http://www.cise.ufl.edu/class/cda5155sp12/projects/Project2/t1.txt) [t1\_sim.txt(Output)](http://www.cise.ufl.edu/class/cda5155sp12/projects/Project2/t1_sim.txt)
* You can also view the [t1\_dis.txt](http://www.cise.ufl.edu/class/cda5155sp12/projects/Project2/t1_dis.txt) for the above input file. This is for your reference only.